High Performance 8A Integrated Power Stage

Features

- **Integrated 8.7mΩ at VCC=5V N-Channel MOSFET for Low Side**
- **Integrated 20mΩ at VCC=5V N-Channel MOSFET for High Side**
- **VCC Power-On-Reset Feature Integrated**
- **Adjustable Over-Current Protection Threshold**
- **Tri-State PWM Input Function**
- **EN Timing Control Function**
- **Adaptive Shoot-Through Protection**
- **Skip Mode Operation**
- **Over Temperature Protection**

Applications

- **Notebook Computers**
- **I/O Supply**
- **Chipset/RAM Supply as Low as 0.8V**
- **Networking Power Supply**

General Description

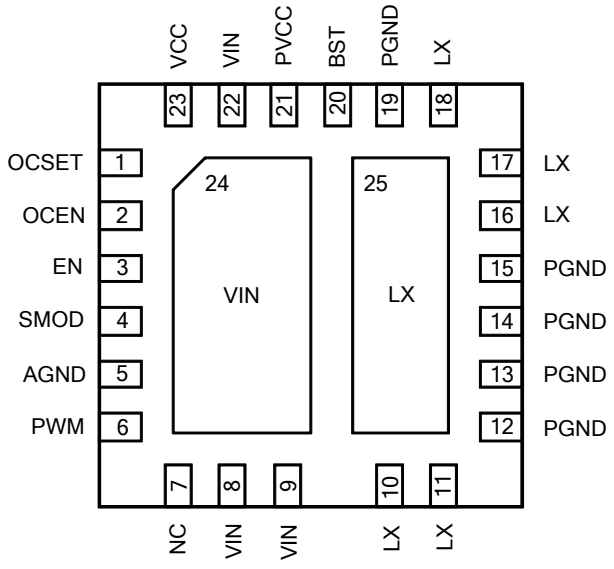
G5421 is a 8A, power stage with integrated 20mΩ N-channel high-side MOSFET and 8.7mΩ N-channel low-side MOSFET. It includes a tri-state PWM input function. When the PWM input signal stays tri-state, the tri-state function turns off the high-side MOSFET and low-side MOSFET. The Power-On-Reset (POR) circuit with hysteresis monitors VCC to start up or shut down the IC. The over-current protection function monitors the output current without the current sensing resistor that achieves high efficiency and low cost. It can be enabled by OCEN pin. The skip mode operation is activated by SMOD pin. The G5421 is available in QFN4X4-23 package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5421QT1U	5421	-40°C to +85°C	QFN4X4-23

Note: QT: QFN4X4-23
1: Bonding Code
U : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



G5421 QFN4X4-23

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

VIN to AGND . . . . . -0.3V to 30V
VCC to AGND . . . . . -0.3V to 6V
PVCC to AGND . . . . . -0.3V to 6V
EN, SMOD, OCSET, PWM to AGND . . . . -0.3V to 6V
BST to PGND . . . . . .-0.3V to 35V
LX to BST. . . . . -6V to 0.3V

Thermal Resistance of Junction to Ambient, (θ_{JA})
QFN4X4-23 . . . . . 25°C/W
Junction Temperature . . . . . .150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 300°C

Electrical Characteristics

(VIN=12V, VCC=5V, PVCC=5V, EN=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN Input Voltage Range	VIN	4.5	---	25	V
VCC Input Voltage Range	VCC	4.5	5	5.5	V
Quiescent Supply Current (VCC)	EN=High, PWM=Low, SMOD=Low, OCEN=High	---	240	270	µA
	EN=High, PWM=Low, SMOD=High, OCEN=Low	---	90	120	µA
Shutdown Current (VCC)	EN=Low	---	---	1	µA
VCC Rising POR Threshold		3.7	4.0	4.3	V
VCC POR Hysteresis		---	200	---	mV
Zero Current Detect	LX - PGND	-10	---	5	mV
OCSET Current Source		9	10	11	µA
Thermal Shutdown Threshold	Hysteresis=45°C	---	145	---	°C
High Side Switch Resistance	BST - LX forced to 5V, VCC=5V	---	20	---	mΩ
Low Side Switch Resistance	VCC=5V	---	8.7	---	mΩ
PWM Input Logic Threshold	PWM Rising ($V_{TH\_PWM\_R}$)	3.6	3.9	4.1	V
	PWM Falling ($V_{TH\_PWM\_F}$)	1.0	1.2	1.4	V
Tri-state Input Rising Logic Threshold	PWM Rising ($V_{TH\_TRI\_R}$)	1.0	1.3	1.6	V
	Hysteresis	140	280	420	mV
Tri-state Input Falling Logic Threshold	PWM Falling ($V_{TH\_TRI\_F}$)	3.4	3.7	4.0	V
	Hysteresis	85	170	255	mV
Logic Input High Voltage	EN, SMOD, OCEN	2.0	---	---	V
Logic Input Low Voltage	EN, SMOD, OCEN	---	---	0.8	V
Tri-state Hold Off Time	t_{TSHO}	---	150	---	ns
Tri-state to High/Low Side ($t_{PD\_TRI\_R}$)	PWM Tri-state to High/Low to DH/DL Low to High	---	20	---	ns
PWM to High side Gate ($t_{PD\_OFF\_DH}$)	PWM High to Low to DH High to Low	---	20	---	ns
PWM to Low side Gate ($t_{PD\_OFF\_DL}$)	PWM Low to High to DL High to Low	---	20	---	ns
Low to High side Gate Deadtime ($t_{PD\_ON\_DH}$)	DL High to Low to DH Low to High	---	20	---	ns
High to Low side Gate Deadtime ($t_{PD\_ON\_DL}$)	DH High to Low to DL Low to High	---	20	---	ns

PWM Timing Diagram

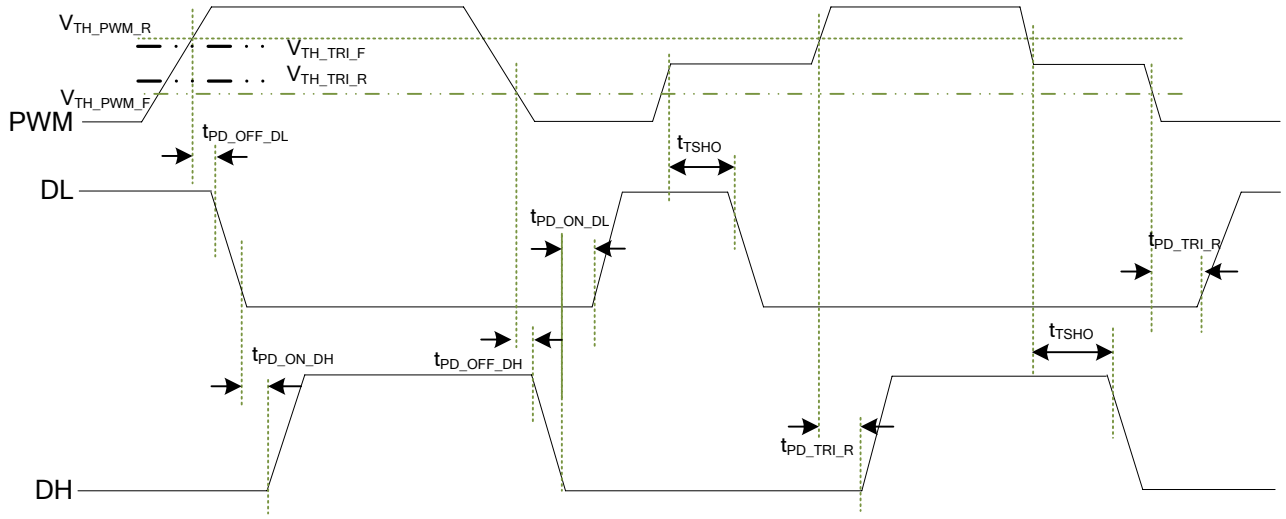


Fig. 1 Definition of PWM Logic and Tri_State

Table 1 Truth Table

EN	SMOD	PWM	DH	DL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	Skip mode
H	X	Tri-state	L	L
H	H	H	H	L
H	H	L	L	H

Pin Description

PIN	NAME	FUNCTION
1	OCSET	Over-Current Setting Input. Connect a resistor to GND to set the OCP trip level.
2	OCEN	OC Enable Pin. Logic high enables the over current protection function. Logic low disables the function. The pin is not floating.
3	EN	Enable Pin. Logic high enables the device. Logic low disables the device. The pin is not floating.
4	SMOD	Skip Mode Input. Pull SMOD low to enter diode emulation or skip mode.
5	AGND	Analog Ground
6	PWM	Control Input for Driver
7	NC	No connection
8,9,22,24	VIN	Power Supply Input.
10,11,16,17,18,25	LX	Junction Point of High-side and Low-side MOSFET. Connect the output LC filter for PWM output voltage.
12,13,14,15,19	PGND	Power Ground.
20	BST	Boost Flying-Capacitor Connection. Connect an external capacitor from BST to LX.
21	PVCC	Supply Voltage Input Pin for Low-side Gate Driver
23	VCC	Analog Supply Input and Supply for Internal Circuits. Place a bypass capacitor from VCC to AGND.

Block Diagram

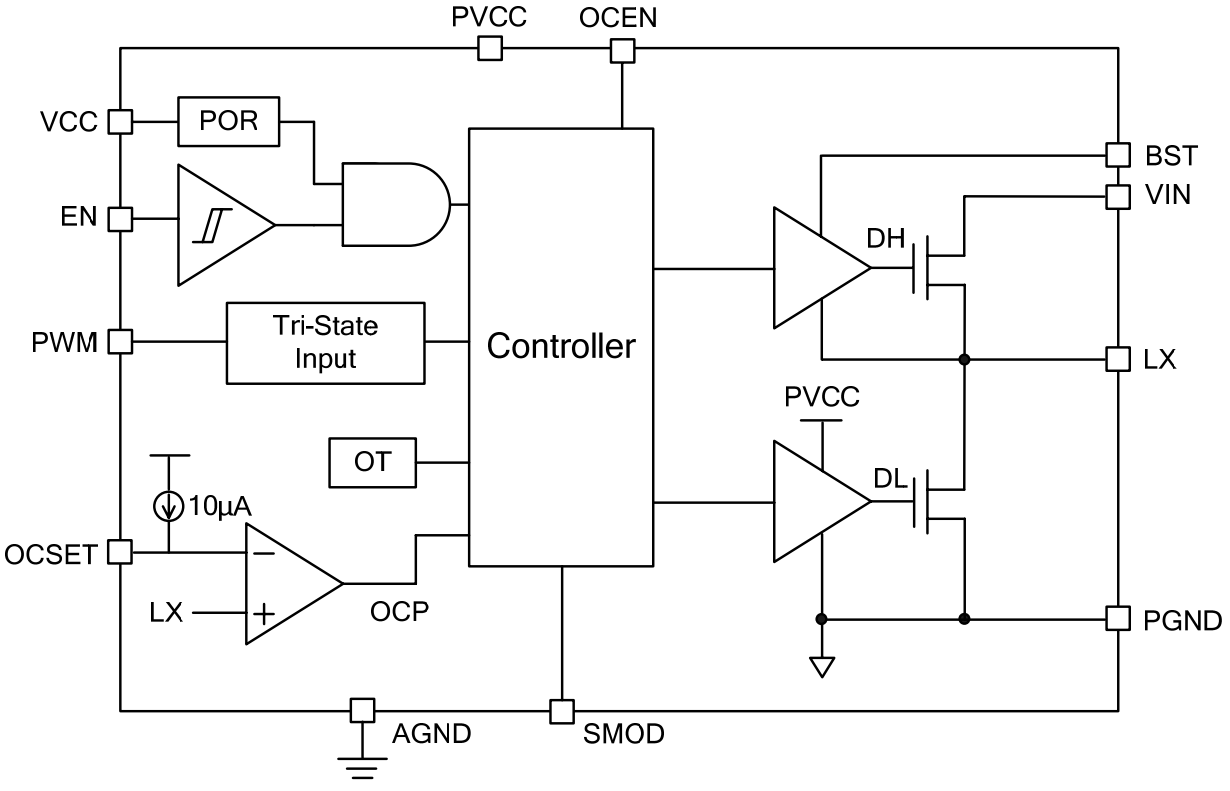


Fig. 2 Block Diagram of G5421

Typical Application Circuit

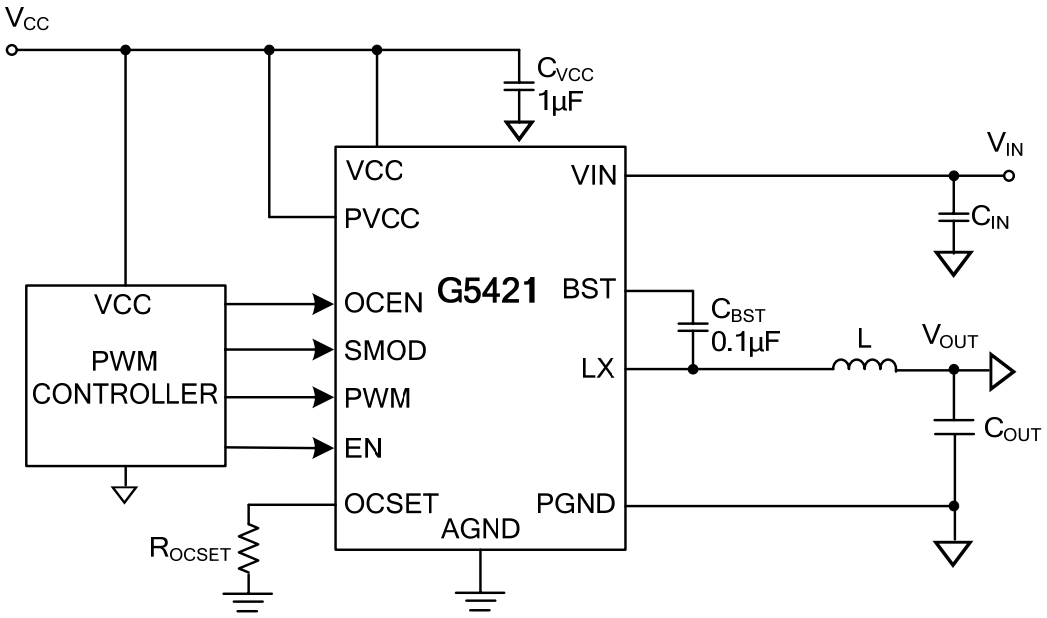


Fig. 3 Application Circuit

Detailed Description

Supply Voltage and Power-On-Reset (POR)

G5421 required a 5V bias supply for the internal PWM circuit and gate-drivers. The POR circuit monitors the supply voltage at the VCC pin. When the VCC supply voltage exceeds the POR rising threshold voltage, the POR circuit enables the device. The POR circuit has a hysteresis and deglitch time so that it will ignore noise on the VCC pin. Bypass VCC to AGND with a capacitor and close to the device.

Enable Control

Pulling the EN pin above 2V will enable the driver output, and pulling EN pin below 0.8V will disable the driver output. If enable function is not used, connect EN to VCC for normal operation.

OC Enable Control

Pulling the OCEN pin above 2V will enable the over current protection function, and pulling OCEN pin below 0.8V will disable the function. If over current protection function is not used, connect OCEN to PGND for normal operation.

Tri-state PWM Input

The PWM pin has three states. When the PWM pin is high level state, the internal pre-driver output of high-side (DH) goes high and internal pre-driver output of low-side (DL) goes low. When the PWM pin is low level state, the DH goes low level and DL goes high level. When the PWM pin is tri-state level, the DH goes low level and DL goes high level.

SMOD

When SMOD is low, G5421 will operate in skip mode. In skip mode, if the PWM is low and ZC is detected, it turns off the low-side switch. This scheme will improve the light-load efficiency. When SMOD is high, G5421 will operate in force PWM mode.

Fault Protection

G5421 provides over-current protection function and over-temperature protection function.

The over-current protection (OCP) function activates when the inductor current is over the internal OCP trip point. The high-side gate driver is latched off.

G5421 has an over-temperature protection (OTP) that occurs when the die temperature is above 145°C. It will shutdown the PWM and force high-side and low-side gate drivers output low.

Output Load Current Limit

G5421 uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current-sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the valley current adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and input voltage. No external current-sensing resistor is necessary in the output current path. An OCSET pin could be used to adjust the current-limit threshold. The R_{OCSET} resistor between OCSET pin and PGND pin sets the threshold. It is connected to a 10 μA current source within G5421. The equation for the current limit threshold is as follows:

$$I_{LIMIT} = \frac{R_{OCSET}}{R_{DS(ON)}} \times 10^{-5} (A)$$

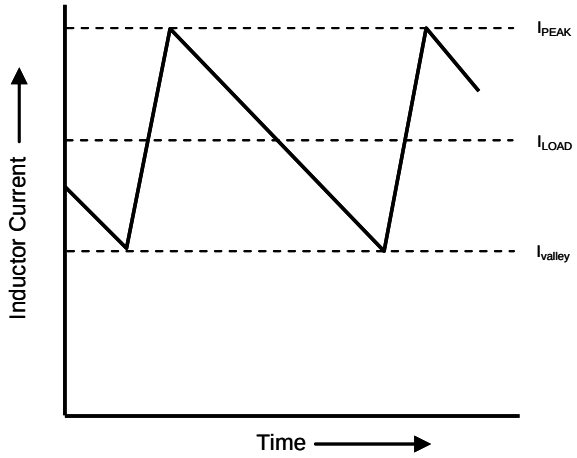
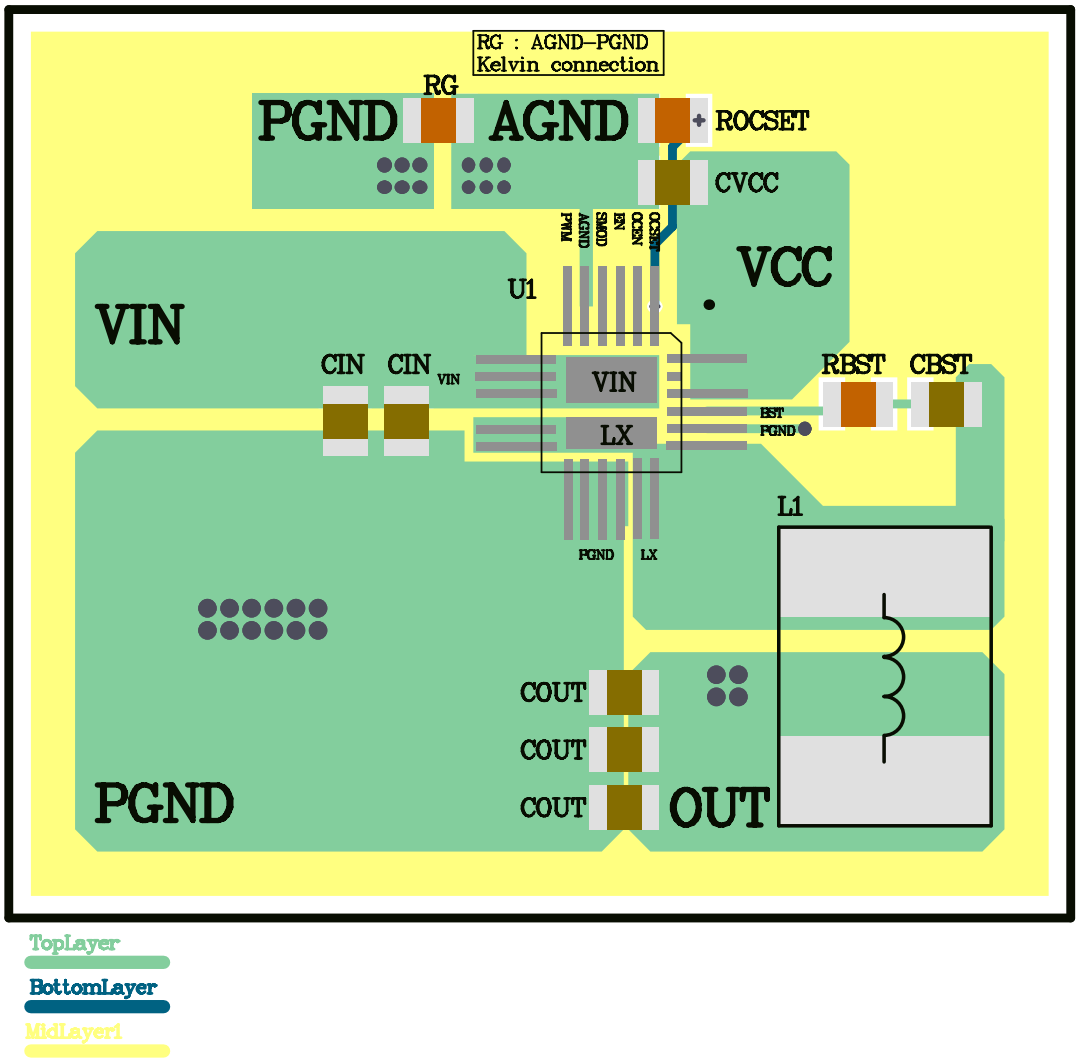


Fig. 4 Output Load Current Limit

Layout Considerations

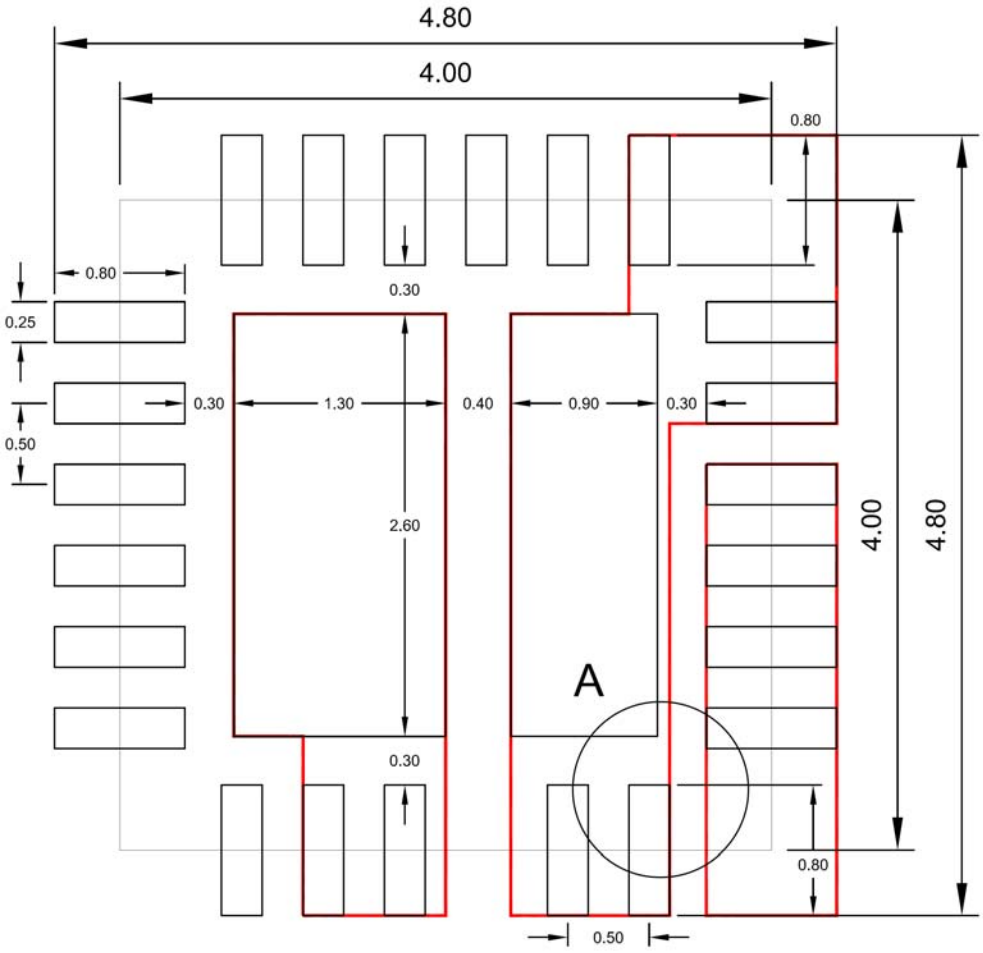
- The input capacitors should be placed close to the VIN pin, and the ground terminals of input capacitors and output capacitors should be close PGND pin.
- To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
- Connect AGND and PGND together close to the IC and the negative terminal of C_{OUT}.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as OUT should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

PCB Layout Guide



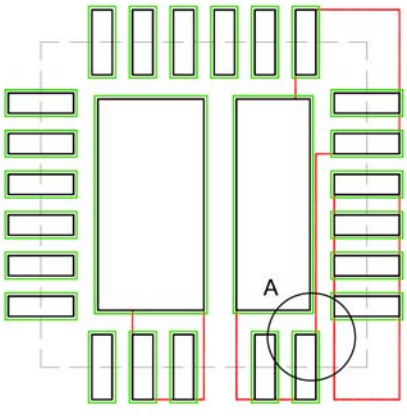
Minimum Footprint PCB Layout Section

QFN4X4-23

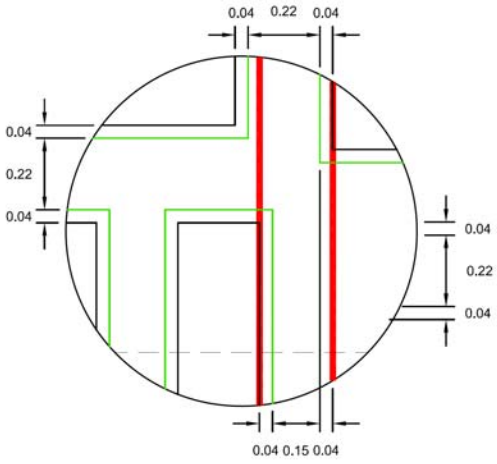


Top Layer

* Recommend Top Layer Thermal Pad Design Following Red Line for Better Characteristic.

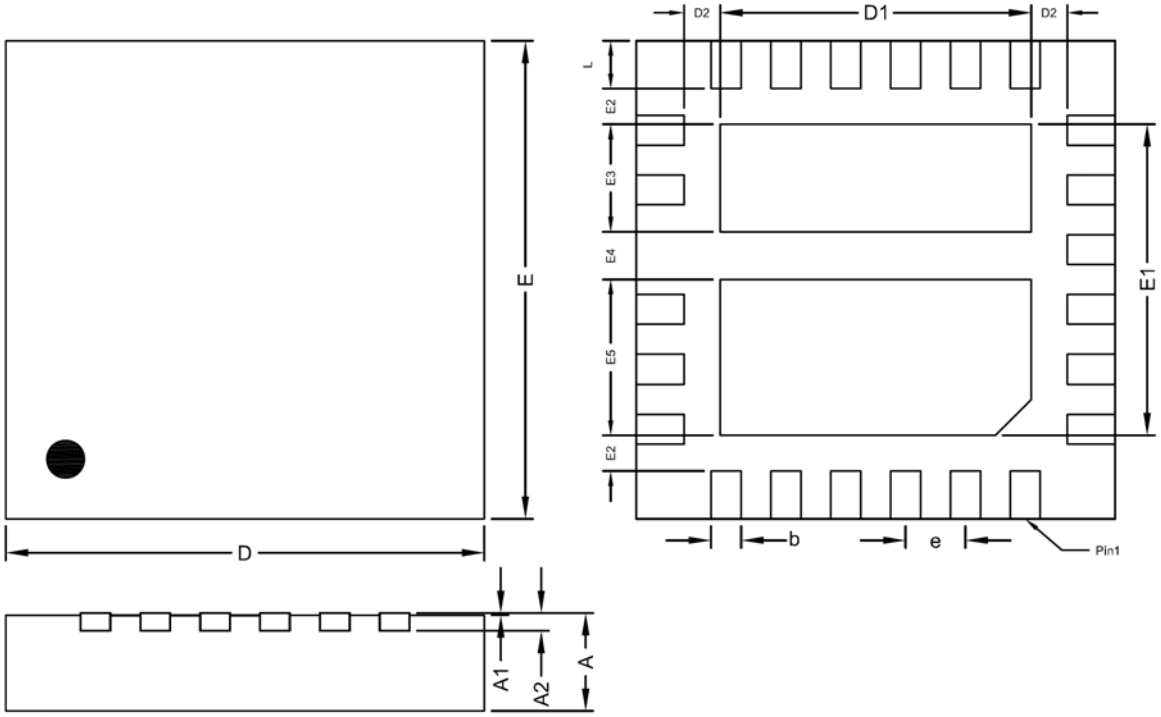


Top Layer with Solder Mask



Section A

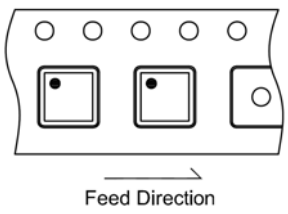
Package Information



QFN4X4-23 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.0000	---	0.0020
A2		0.20 REF			0.0079 REF	
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.50	2.60	2.70	0.0984	0.1023	0.1063
E1	2.50	2.60	2.70	0.0984	0.1023	0.1063
D2		0.30 BSC			0.0118 BSC	
E2		0.30 BSC			0.0118 BSC	
E3	0.85	0.90	0.95	0.0335	0.0354	0.0374
E4	0.35	0.40	0.45	0.0138	0.0157	0.0177
E5	1.25	1.30	1.35	0.0492	0.0512	0.0531
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
e		0.50 BSC			0.0197 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN4X4-23	3,000 ea